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TITLE: **INTERLEAVING AD CONVERSION TYPE WAVEFORM DIGITIZER**

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INTERLEAVING AD CONVERSION TYPE WAVEFORM DIGITIZER

[0001] The present application is a continuation application of PCT application No. PCT/JP02/01429 filed on February 19, 2002 which claims priority from a Japanese Patent Application No. 2001-44078 filed on February 20, 2001, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an interleaving AD conversion type waveform digitizer. In particular, the present invention relates to a correction means for detecting a measurement error caused by a phase error of a sampling timing in interleaving AD conversion so as to correct the detected measurement error.

Related Art

[0003] An N-way interleaving AD conversion type waveform digitizer can increase an apparent sampling rate by using N A/D converters. This type of waveform digitizer is required to perform sampling at precise timings.

[0004] Fig. 7 shows a structure of a conventional digitizer 200 used in a testing apparatus for testing an electronic device. The digitizer 200 includes four A/D converters (ADCs) 110, four clocks 112, an interleaving unit 114 and a digital filter 116. Each A/D converter 110 samples an analog signal output from the electronic device based on timings supplied to the associated clock 112, thereby converting the analog signal to a digital signal. The interleaving unit 114 generates a data sequence

obtained by arranging the digital signals converted by the four A/D converters 110 in a predetermined order. The digital filter 116 multiplies the data sequence generated by the interleaving unit 114 by a correction coefficient based on a predetermined impulse response function. The digital filter 116 removes a predetermined frequency component from the data sequence by the above multiplication. Then, the digital filter 116 outputs the data sequence multiplied by the correction coefficient to a determination unit of the testing apparatus. The determination unit determines based on the data sequence multiplied by the correction coefficient whether or not the electronic device is defective.

[0005] The four A/D converters have to be adjusted in phase in such a manner that the sampling timings thereof are arranged at constant phase intervals. In a case where the sampling timings of the respective A/D converters contain phase errors, the interleaving unit 114 and the digital filter 116 process the digital data output from the respective A/D converters while assuming that that digital data were obtained by sampling at constant intervals. As a result, the data sequence output from the digital filter 116 also contains an error with respect to the analog signal output from the electronic device. Therefore, the determination unit cannot precisely determine whether or not the electronic device under test is defective.

[0006] According to the conventional technique, the phase intervals between the sampling timings of the A/D converters were adjusted to be constant, as described above. On the other hand, the sampling characteristics of the A/D converter are affected by variation of parts in the A/D converter, the environmental temperature, the change with time, the fluctuation of supply voltage, thus affecting the sampling at constant

intervals that is intended. Moreover, it was very difficult to supply clocks to a plurality of A/D converters so as to realize the sampling timings at constant phase intervals. These factors cause the fluctuation of the sampling timing from ideal sampling timing. This made it difficult to precisely reproduce the analog signal output from the electronic device. Thus, it became difficult to precisely determine whether or not the electronic device is defective.

SUMMARY OF THE INVENTION

[0007] Therefore, it is an object of the present invention to provide an AD conversion type digitizer and a semiconductor testing apparatus that can correct phase shifts of sampling between a plurality of A/D converters so as to precisely reproduce an analog signal. The above and other objects can be achieved by combinations described in the independent claims. The dependent claims define further advantageous and exemplary combinations of the present invention.

[0008] In order to achieve the above object, according to the first aspect of the present invention, a digitizer for converting an analog signal output from an electronic device to a digital signal, includes: an A/D converter operable to sequentially convert the analog signal output from the electronic device to a digital signal at predetermined time intervals; a digital filter operable to output a corrected signal obtained by multiplying the digital signal converted by the A/D converter by a correction coefficient; and a digital filter operable to output a corrected signal obtained by multiplying the digital signal converted by the A/D converter by a correction coefficient based on a phase error between an ideal sampling timing at which

the A/D converter is to sample the analog signal and an actual timing at which the A/D converter sampled the analog signal.

[0009] The digital filter may have an impulse response function given thereto for calculating the correction coefficient, and the digital filter may output the corrected signal obtained by calculating convolution of the correction coefficient, that is a value of the impulse response function corresponding to a timing away from the ideal sampling timing by the phase error, and values of the digital signal.

[0010] According to the second aspect of the present invention, a digitizer for converting an analog signal output from an electronic device to a digital signal, includes: N A/D converters operable to convert the analog signal output from the electronic device to digital signals at different sampling timings by turns, N being an integer equal to or larger than 2; and N digital filters operable to output corrected signals, each of the corrected signals being obtained by multiplying one of the digital signals output from an associated one of the N A/D converters by a correction coefficient based on a phase error between an ideal sampling timing at which the associated A/D converter is to sample the analog signal and an actual sampling timing at which the associated A/D converter sampled the analog signal.

[0011] Each of the N digital filters may include a memory in which an impulse response function for calculating the correction coefficient is stored, and the N digital filters may output the corrected signals each obtained by calculating convolution of the correction coefficient, that is a value of the impulse response function corresponding to a timing away from the ideal sampling timing by the phase error of the associated A/D converter, and values of the digital signal converted by

the associated A/D converter. In addition, the memory may store the impulse response function based on gain characteristics of the associated A/D converter. Moreover, the memory may store the impulse response function based on frequency characteristics of the associated A/D converter.

[0012] Each of the N digital filters may include a memory for storing as the correction coefficient a value of an impulse response function of the digital filter at the actual sampling timing of the associated A/D converter, and the N digital filters may output the corrected signals each obtained by calculation of convolution of values of the digital signal converted by the associated A/D converter and the correction coefficient. In addition, the memory may store the correction coefficient based on gain characteristics of the associated A/D converter. Moreover, the memory may store the correction coefficient based on frequency characteristics of the associated A/D converter.

[0013] The digitizer may further include an interleaving unit operable to generate a data sequence obtained by arranging the corrected signals respectively output from the N digital filters in a predetermined order. Moreover, the digitizer may further include a decimation data generation unit operable to calculate a sum of the corrected signals respectively output from the plurality of digital filers to generate decimation data, wherein each of the N digital filters multiplies the digital signal output from the associated A/D converter by the correction coefficient based on: a phase error between the ideal sampling timing at which the associated A/D converter is to sample the analog signal and the actual sampling timing at which the associated A/D converter sampled the analog signal; and a phase difference between the ideal sampling timing of the associated A/D converter and an ideal sampling timing of one of the N A/D

converters that is used as a reference A/D converter.

[0014] Each of the N digital filters may include a memory for storing a plurality of correction coefficients obtained by decomposing a predetermined impulse response function by a polyphase decomposition and multiplying results of the polyphase decomposition by a coefficient based on the phase error, and the N digital filters may output the corrected signals obtained by calculation of convolution of the plurality of correction coefficients and the digital signals. Moreover, the memory of each of the N digital filters may store, as the plurality of correction coefficients, values obtained by multiplying values of the impulse response function at the ideal sampling timings of the associated A/D converter by the coefficient based on the phase error. Furthermore, the memory of each of the N digital filters may store the plurality of correction coefficients based on a function obtained by moving the impulse response function on a time axis by a difference between a phase of the ideal sampling timing of the associated A/D converter and a phase of the ideal sampling timing of the reference A/D converter, and the phase error.

[0015] According to the third aspect of the present invention, a digitizer for converting an analog signal output from an electronic device to a digital signal, includes: N A/D converters operable to convert the analog signal output from the electronic device to digital signals at different sampling timings by turns, N being an integer equal to or larger than 2; a first interleaving unit operable to generate a first data sequence obtained by arranging the digital signals converted by the N A/D converters in a predetermined order to output the first data sequence; N digital filters operable to receive the first data sequence output from the first interleaving unit,

to calculate convolution of correction coefficients based on phase errors between ideal sampling timings at which the N A/D converters are to sample the analog signal and actual sampling timings at which the N A/D converters sampled the analog signal and the first data sequence so that each of the N digital filters generate and output decimation data containing less number of data units than data units in the first data sequence; and a second interleaving unit operable to generate a second data sequence obtained by arranging the data units in the decimation data output from each of the N digital filters in a predetermined order.

[0016] In the third aspect of the present invention, the N digital filters may include memories operable to store impulse response functions for calculating the correction coefficients, and may output signals obtained by convolution of values of the impulse response functions corresponding to timings away from the ideal sampling timings by the phase errors of associated A/D converters and values of the digital signals converted by the associated A/D converters, respectively.

[0017] According to the fourth aspect of the present invention, a testing apparatus for testing an electronic device, includes: a pattern generator operable to generate a pattern signal and an expected-value signal; a waveform shaping unit operable to shape a waveform of the pattern signal generated by the pattern generator; a device contact unit, onto which the electronic device is to be placed, operable to supply the pattern signal shaped by the waveform shaping unit to the electronic device and to receive an analog signal output from the electronic device; a digitizer operable to convert the analog signal output from the electronic device to a digital signal; and a determination unit operable to determine based on the

expected-value signal output from the pattern generator and a signal output from the digitizer whether or not the electronic device is defective, wherein the digitizer includes: an A/D converter operable to sequentially convert the analog signal output from the electronic device to digital signals at predetermined intervals; and a digital filter operable to output corrected signals calculated by multiplying the digital signals converted by the A/D converter by a correction coefficient, and the digital filer multiplies the digital signals by the correction coefficient based on a phase error between ideal sampling timings at which the A/D converter is to sample the analog signal and sampling timings at which the A/D converter sampled the analog signal.

[0018] According to the fifth aspect of the present invention, a testing apparatus for testing an electronic device, includes: a pattern generator operable to generate a pattern signal and an expected-value signal; a waveform shaping unit operable to shape a waveform of the pattern signal generated by the pattern generator; a device contact unit, onto which the electronic device is to be placed, operable to supply the pattern signal shaped by the waveform shaping unit to the electronic device and to receive an analog signal output from the electronic device; a digitizer operable to convert the analog signal output from the electronic device to a digital signal; and a determination unit operable to determine based on the expected-value signal output from the pattern generator and a signal output from the digitizer whether or not the electronic device is defective, wherein the digitizer includes: N A/D converters operable to convert the analog signal output from the electronic device to digital signals at different sampling timings, N being an integer equal to or larger than 2; and N

digital filters operable to output corrected signals obtained by multiplying the digital signals output from the N A/D converters by correction coefficients, and wherein the N digital filters multiply the digital signals converted by associated A/D converters by the correction coefficients based on phase errors between ideal sampling timings at which the associated A/D converters are to sample the analog signal and sampling timings at which the N A/D converters sampled the analog signal.

[0019] The digitizer may further include a decimation data generation unit operable to calculate a sum of the corrected signals respectively output from the plurality of digital filters to generate decimation data, wherein the N digital filters output the corrected signals obtained by multiplying the digital signals converted by the associated A/D converters by the correction coefficients based on: phase errors between the ideal sampling timings at which the associated A/D converters are to sample the analog signal and the actual sampling timing at which the N A/D converters sampled the analog signal; and phase differences between the ideal sampling timings of the associated A/D converters and ideal sampling timings of one of the N A/D converters that is used as a reference.

[0020] According to the sixth aspect of the present invention, a testing apparatus for testing an electronic device includes: a pattern generator operable to generate a pattern signal and an expected-value signal; a waveform shaping unit operable to shape a waveform of the pattern signal generated by the pattern generator; a device contact unit, onto which the electronic device is to be placed, operable to supply the pattern signal shaped by the waveform shaping unit to the electronic device and to receive an analog signal output from the electronic device; a digitizer operable to convert the analog signal output

from the electronic device to a digital signal; and a determination unit operable to determine based on the expected-value signal output from the pattern generator and a signal output from the digitizer whether or not the electronic device is defective, wherein the digitizer includes: N A/D converters operable to convert the analog signal output from the electronic device to digital signals at different sampling timings by turns, N being an integer equal to or larger than 2; a first interleaving unit operable to generate and output a first data sequence obtained by arranging the digital signals converted by the N A/D converters in a predetermined order; N digital filters operable to receive the first data sequence output from the first interleaving unit and to calculate convolution of correction coefficients, based on phase errors between ideal sampling timings at which the N A/D converters are to sample the analog signal and actual sampling timings at which the N A/D converters sampled the analog signal, and the first data sequence to generate and output decimation data, the decimation data of each of the N digital filters containing less number of data units than data units in the first data sequence; and a second interleaving unit operable to generate a second data sequence obtained by arranging the data units in the decimation data output from the N digital filters in a predetermined order.

[0021] The summary of the invention does not necessarily describe all necessary features of the present invention. The present invention may also be a sub-combination of the features described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Fig. 1 shows an exemplary structure of a testing apparatus 100 according to the present invention.

[0023] Fig. 2 shows an exemplary structure of a digitizer 50 according to the present invention.

[0024] Fig. 3 shows a waveform of an impulse response function stored in a memory of a digital filter 56 and sampling timings of A/D converters 52.

[0025] Fig. 4 shows another exemplary structure of the digitizer 50 according to the present invention.

[0026] Fig. 5 shows an exemplary impulse response function of each digital filter 56.

[0027] Fig. 6 shows still another example of the structure of the digitizer 50 according to the present invention.

[0028] Fig. 7 shows a structure of a conventional digitizer 200.

DETAILED DESCRIPTION OF THE INVENTION

[0029] The invention will now be described based on the preferred embodiments, which do not intend to limit the scope of the present invention, but exemplify the invention. All of the features and the combinations thereof described in the embodiment are not necessarily essential to the invention.

[0030] Fig. 1 shows an exemplary structure of a testing apparatus 100 according to the present invention. The testing apparatus 100 includes a pattern generator 10, a waveform shaping unit 20, a device contact unit 30, a digitizer 50 and a determination unit 40. An electronic device 60 under test is placed onto the device contact unit 30. The pattern generator 10 generates an input signal to be supplied to the electronic device 60. The input signal thus generated is supplied to the

waveform shaping unit 20. The waveform shaping unit 20 shapes the waveform of the input signal in accordance with the characteristics of the electronic device 60. The shaped input signal is supplied to the electronic device 60 via the device contact unit 30. The electronic device 60 outputs based on the input signal an analog signal to the digitizer 50 via the device contact unit 30. The digitizer 50 receives the analog signal and converts the received analog signal to a digital signal so as to supply the digital signal to the determination unit 40. The determination unit 40 determines based on the digital signal whether or not the electronic device 60 is defective. The pattern generator 10 may generate an expected-value signal based on the input signal that the pattern generator 10 generates, while the determination unit 40 may compare the expected-value signal generated by the pattern generator 10 with the digital signal received from the digitizer 50 so as to determine whether or not the electronic device 60 is defective.

[0031] Fig. 2 shows an exemplary structure of the digitizer 50 according to the present invention. The digitizer 50 includes N (N is an integer) A/D converters (ADCs) 52, digital filters 56 respectively corresponding to the A/D converters 52, clocks 54 each of which supplies sampling timings to the associated one of the A/D converters 52, and an interleaving unit 58. In the present example, the digitizer 50 includes four A/D converters 52.

[0032] The N A/D converters 52 convert the analog signal out put from the electronic device 60 to digital signals at different sampling timings by turns. Each of the N A/D converters 52 samples the analog signal at substantially the same frequency (fs). In the present example, the A/D converter 52a, the A/D converter 52b, the A/D converter 52c and the A/D converter 52d

sample the analog signal by turns. Thus, by sampling the analog signal at constant phase intervals by means of these four A/D converters 52, the frequency of the sampling by the four A/D converters 52 is 4fs. However, since the four A/D converters 52 perform the sampling by turns, the phase intervals between the sampling timings are not constant in some cases. That is, the sampling timings at which the N A/D converters 52 sample the analog signal contain phase errors with respect to ideal sampling timings arranged at constant phase intervals. In the present example, in a case where the timing of the sampling by the A/D converter 52a is assumed to be reference, it is ideally desirable that the other A/D converters 52b, 52c and 52d perform the sampling at constant phase intervals between adjacent sampling timings of the A/D converter 52a. However, the sampling timings of the A/D converters 52b, 52c and 52d may contain the phase errors with respect to the ideal sampling timings actually.

[0033] Each digital filter 56 multiplies the digital signal output from the associated A/D converter 52 by a correction coefficient for correcting the phase error. In other words, the N digital filters 56 multiply the digital signals output from the N A/D converters 52 corresponding thereto by correction coefficients so as to obtain corrected signals, respectively, and then output the obtained corrected signals to the interleaving unit 58. In this multiplication, each correction coefficient is based on the phase error between the ideal sampling timings at which the associated A/D converter 52 is to sample the analog signal and actual sampling timings at which the respective N A/D converters 52 sampled the analog signal. The digital filter 56 may be a finite impulse response (FIR) filer, for example. Moreover, it is preferable that the digital filter 56 is a linear-phase finite impulse response filter and is a

filter having characteristics freely changeable.

[0034] The interleaving unit 58 generates a data sequence that is obtained by arranging the corrected signals respectively output from the N digital filters 56 in a predetermined order. That is, the interleaving unit 58 does not change the order of data units in data series of each corrected signal but arranges data units of the corrected signals in a predetermined order, thereby generating the data sequence.

[0035] The N digital filters 56 may include memories in which impulse response functions for calculating the correction coefficients of the respective digital filters 56 are stored. In this case, it is preferable that each of the N digital filters 56 outputs the corrected signal obtained by calculating convolution of the correction coefficient, that is a value of the impulse response function corresponding to the time away from the ideal sampling timing of the associated A/D converter by the phase error of the associated A/D converter, and a value of the digital signal converted by the associated A/D converter 52. Next, an exemplary method for calculating the corrected signal in the digital filter 56 is described.

[0036] Fig. 3 shows a waveform of the impulse response function stored in the memory of the digital filter 56 and the sampling timings of the A/D converters 52. In Fig. 3, the horizontal axis represents time while the vertical axis in the part showing the waveform of the impulse response function represents the gain of the digital filter 56. In the present example, a case where four A/D converters 52 are provided, as shown in Fig. 2, and the impulse response functions of the digital filters 56 are the same is described. An ideal sampling timing part shows the ideal sampling timings at which the four A/D converters 52 are to sample the analog signal output from the

electronic device 60. A 52a-sampling timing part shows the actual sampling timings at which the A/D converter 52a in Fig. 2 actually samples the analog signal; a 52b-sampling timing part shows the actual sampling timings at which the A/D converter 52b in Fig. 2 actually samples the analog signal; a 52c-sampling timing part shows the actual sampling timings at which the A/D converter 52c in Fig. 2 actually samples the analog signal; and a 52d-sampling timing part shows the actual sampling timings at which the A/D converter 52d in Fig. 2 actually samples the analog signal.

[0037] As described above, in some cases the actual sampling timings at which the N A/D converters 52 actually sample the analog signal contain the phase errors with respect to the ideal sampling timings. In the present example, when the sampling timing of the A/D converter 52a is used as reference, the actual sampling timings of the A/D converters 52b, 52c and 52d contain the phase errors of τ_1, τ_2 and τ_3 with respect to the ideal sampling timings, respectively. The digital filter 56 outputs the corrected signal obtained by calculating convolution of the correction coefficient, that is a value of the impulse response function corresponding to the timing away from the ideal sampling timing by the phase error of the associated A/D converter 52, and a value of the digital signal converted by the associated A/D converter 52. That is, the digital filter 56 outputs the corrected signal obtained by calculating convolution of the digital signal output from the associated A/D converter 52 and the value of the impulse response function at the actual sampling timing of the associated A/D converter 52. It is preferable that the phase error of each A/D converter is given in advance. The phase error of each A/D converter can be easily calculated, for example, based on the result of sampling

of a predetermined analog signal. Next, convolution operation in the digital filter 56 is described.

[0038] It is assumed that a data series output from the A/D converter 52 is x(n) and a value of the impulse response function of the associated digital filter 56 at the actual sampling timing of that A/D converter 52 is represented by h(n). In this case, the corrected signal output from the associated digital filter 56, y(n), is represented by the following expression. The number of data units included in the data series x(n) and the number of the data units included in h(n) may be the same.

[0039] $$y(n) = \sum_{m=0}^{N-1} x(m)h(n-m)$$

[0040] In the above expression, N represents the number of the data units included in h(n). Moreover, it is preferable to determine the number of the data units included in the data series x(n) of the digital signal that was output from the A/D converter 52 and was then input to the digital filter 56 based on the sampling frequency fs of the A/D converter 52 and the impulse response function. According to the digitizer described above, the operation for correction in the digital filter 56 is performed using the correction coefficient based on the phase error in the actual sampling timing of the A/D converter 52. Thus, it is possible to generate the corrected signal in which the phase error has been corrected and is also possible to precisely reproduce the analog signal output from the electronic device 60. In addition, according to the testing apparatus 100 of the present invention, it is possible to precisely determine whether or not the electronic device 60 is defective. Moreover, although the digitizer 50 including four A/D converters 52 has been described in the present example,

it is apparent that, in a digitizer including N A/D converters 52, it is also possible to generate the corrected signals in which the phase errors have been corrected and to precisely reproduce the analog signal by performing the similar operation to the operation described in the present example.

[0041] In the present example, the N digital filters 56 store the same impulse response function in the memories of the respective digital filters 56. However, in an alternative example, the memory of each digital filter 56 may store the impulse response function based on the gain characteristics of the associated A/D converter 52. In other words, it is preferable that the memories of the digital filters 56 store the impulse response functions that correct the difference between the gain characteristics of the N A/D converters 52, respectively. Moreover, the memory of each digital filter 56 may store the impulse response function based on the frequency characteristics of the associated A/D converter 52. In other words, it is preferable that the digital filter 56 store the impulse response function that corrects the difference of the gain characteristics between the frequencies in the associated A/D converter 52.

[0042] In the present example, the memories of the N digital filters store the impulse response functions, respectively. However, in an alternative example, the memories of the N digital filters may store the correction coefficients calculated based on the impulse response functions. For example, the memory of the digital filter may store a table of correction coefficients calculated by the above-mentioned operation, respectively. Moreover, the memory of the digital filter may store a table of correction coefficients corresponding to a plurality of phase errors or actual sampling timings in advance. That is, each of the N digital filters 56 may include a memory for storing,

as a correction coefficient, a value in the impulse response function representing the characteristics of that digital filter 56 at the actual sampling timing of the associated A/D converter 52. The memory preferably stores a table of correction coefficients corresponding to a plurality of actual sampling timings. In this case, each of the N digital filters 56 outputs the corrected signal obtained by calculating convolution of the values of the digital signal of the associated A/D converter 52 and the table of correction coefficients selected based on the phase error or actual sampling timing.

[0043] Moreover, also in the case where the memory stores the correction coefficient table, it is preferable that the memory store the correction coefficient based on the gain characteristics of the associated A/D converter 52 as in the case where the memory stores the impulse response function. In addition, it is preferable that the memory store the correction coefficient based on the frequency characteristics of the associated A/D converter 52.

[0044] Fig. 4 shows another exemplary structure of the digitizer 50 according to the present invention. In Fig. 4, the components labeled with the same reference numerals as those appearing in Fig. 2 may have the same or similar functions and structures as/to the components described referring to Figs. 2 and 3. In this example, the digitizer 50 includes four A/D converters 52, clocks 54 that supply timings to the A/D converters 52, respectively, digital filters 56 respectively corresponding to the A/D converters 52 and a decimation data generation unit 62. The A/D converters 52 and the clocks 54 have the same or similar functions and structures as/to the A/D converters 52 and the clocks 54 described referring to Figs. 2 and 3.

[0045] The digital filter 56 outputs a corrected signal

obtained by multiplying a digital signal converted by the associated A/D converter 52 by a correction coefficient based on a phase error between an ideal sampling timing at which the associated A/D converter 52 is to sample the analog signal and an actual sampling timing at which the associated A/D converter 52 actually sampled the analog signal and a phase difference between the ideal sampling timing of the associated A/D converter 52 and an ideal sampling timing of the A/D converter 52 that is used as reference. In other words, the digital filter 56 corrects the digital signal from the associated A/D converter 52 with the phase error in the associated A/D converter 52 and also converts the digital signal after the correction into a signal sampled at different sampling timings, so as to output the resultant signal as the corrected signal. For example, it is assumed that the ideal sampling timings of the A/D converter 52a at which the A/D converter 52a should sample the analog signal are T_1, T_5, T_9, ... and the ideal sampling timings of the A/D converter 52b at which the A/D converter 52b should sample the analog signal are T_2, T_6, T_{10}, ... In this case, the digital filter 56b converts in phase the digital signal sampled by the A/D converter 52b at the timings of T_2, T_6, T_{10}, ... to a digital signal sampled at the timings of T1, T5, T9, ... and also corrects the phase error in the A/D converter 52b with respect to the ideal sampling timings.

[0046] The decimation data generation unit 62 calculates the sum of the corrected signals respectively output from the digital filters 56 to generate decimation data. More specifically, the decimation data generation unit 62 calculates the sum of the corrected signals which have been subjected to phase conversion in the respective digital filters 56, thereby generating decimation data equivalent to a digital signal sampled

at a lower frequency than the sampling frequency at which the N A/D converters 52 actually sampled the analog signal. The decimation data generation unit 62 outputs the thus generated decimation data to the determination unit 40. Next, the operations of the digital filter 56 and decimation data generation unit 62 are described.

[0047] Fig. 5 shows exemplary impulse response functions of the respective digital filters 56. The four A/D converters 52 ideally sample the analog signal by turns at constant intervals (ΔT) as shown in Fig. 5. However, there may exist phase errors between the actual sampling timings at which the four A/D converters 52 actually sample the analog signal and the ideal sampling timings. In the present example, while the actual sampling timing at which the A/D converter 52a performs the sampling is assumed to be reference, the A/D converters 52b, 52c and 52d have the phase errors of τ_1, τ_2 and τ_3, respectively, with respect to the ideal sampling timing.

[0048] The four digital filters 56 corresponding to the four A/D converters 52 have impulse response functions given thereto, and correct the digital signals output from the associated A/D converters 52 based on the impulse response functions, respectively. To each of the four digital filters 56, a function is given that is obtained by moving the impulse response function on the time axis by a difference between the phase of the ideal sampling timing of the associated A/D converter 52 and the phase of the ideal sampling timing of the A/D converter 52 used as reference. In the present example, to each of the four digital filters 56, the impulse response function is given that is obtained by moving the impulse response function of the A/D converter 52a on the time axis in the negative direction by a phase difference between the ideal sampling timing of the

associated A/D converter 52 and the ideal sampling timing of the A/D converter 52a. Each digital filter 56 calculates convolution of the value of the given impulse response function at the ideal sampling timing of the associated A/D converter 52 and the digital signal output from the associated A/D converter 52.

[0049] In the present example, the digital filter 56a calculates convolution of the values of the impulse response function at the ideal sampling timings, P_n, P_{n+4}, ... and the digital signal, as shown in Fig. 5. P_n, P_{n+4}, ... are the values of the impulse response function appearing at the intervals of $4\Delta T$. Similarly, the digital filter 56b calculates convolution of the values of the impulse response function at the ideal sampling timing, P_{n-3}, P_{n+1}, ... and the digital signal. The digital filters 56c and 56d also calculate convolution of the values of the impulse response functions at the ideal sampling timings and the digital signals similarly.

[0050] Each digital filter 56 multiplies the result of convolution by a coefficient based on a phase error of the associated A/D converter. In a case where the phase errors of the A/D converters 52b, 52c and 52d are assumed to be τ_1, τ_2 and τ_3, respectively, the digital filter 56b multiplies the result of convolution by $e^{(jw\tau_1)}$; the digital filter 56c multiplies the result of convolution by $e^{(jw\tau_2)}$; and the digital filter 56d multiplies the result of convolution by $e^{(jw\tau_3)}$. In this manner, the digital filters 56b, 56c and 56d output corrected signals in which the phase errors have been corrected.

[0051] Since each digital filter 56 has an impulse response function given thereto which is obtained by moving the impulse response function on the time axis by the phase difference between the ideal sampling timing of the associated A/D converter 52

and the ideal sampling timing of the reference A/D converter 52, the digital filter 56 can convert in phase the digital signal sampled by the associated A/D converter 52 to a digital signal sampled at the ideal sampling timings of the reference A/D converter 52. In the present example, the digital filers 56 convert in phase the digital signals sampled by the associated A/D converters 52 to digital signals sampled by the ideal sampling timings of the A/D converter 52a, respectively. The decimation data generation unit 62 calculates the sum of the corrected signals, i.e., the digital signals that are obtained by phase conversion and are output from the digital filters 56, so that the decimation data generation unit 62 can convert the digital signal sampled at the frequency of 4fs by interleaving sampling of the analog signal with the four A/D converters 52 to a digital signal sampled by the frequency of fs and correct the phase errors of the A/D converters 52.

[0052] In the present example, one of the A/D converters 52 is used as the reference and the digital signals sampled by the other A/D converters 52 are subjected to phase conversion. However, in an alternative example, a plurality ones of the A/D converters 52 may be used as the reference and the digital signals sampled by the remaining A/D converters may be subjected to phase conversion. For example, when a case is considered where the A/D converters 52a and 52c are used as the reference, the digital signal output from the A/D converter 52b may be converted in phase to a digital signal at the ideal sampling timings of the A/D converter 52a, and the digital signal output from the A/D converter 52d may be converted in phase to a digital signal at the ideal sampling timings of the A/D converter 52c. In this case, it is possible to convert the digital signal sampled with the four A/D converters 52 at the sampling frequency of 4fs to

a digital signal sampled at the sampling frequency of 2fs. In addition, although the digitizer 50 including the four A/D converters 52 has been described in the present example, it is also possible in a digitizer 50 including N A/D converters 52 to convert a digital signal sampled at the sampling frequency of Nfs with the N A/D converters 52 to a digital signal having the sampling frequency equal to a given integral multiple of the sampling frequency fs of a single A/D converter 52. That is, according to the digitizer 50 of the present invention, a multi-rate digitizer can be realized that can sample the analog signal output from the electronic device 60 at a given frequency and can correct the phase errors in the respective A/D converters 52.

[0053] The digital filters 56 in the present example may have the impulse response functions based on the gain characteristics and/or the frequency characteristics of the associated A/D converters 52 as is the case with the digital filters 56 described referring to Figs. 2 and 3. Moreover, the digital filters 56 may include memories for storing the impulse response functions, respectively. Furthermore, the digital filters 56 may include memories for storing tables of correction coefficients based on the impulse response functions in advance. That is, the memory of each of the N digital filters 56 may store, as a plurality of correction coefficients, valued obtained by multiplying values of the impulse response function at the ideal sampling timings of the associated A/D converter 52 by the coefficient based on the phase error.

[0054] For example, the N digital filters 56 may include memories for storing correction coefficients obtained by decomposing a predetermined impulse response function by polyphase decomposition and multiplying the result of the

polyphase decomposition by coefficients based on the phase errors of the associated A/D converters 52, respectively. For example, in a case where the digitizer 50 includes four digital filters 56, an impulse response is given to each digital filter 56, which is obtained by decomposing a predetermined impulse response function K(z) by polyphase decomposition in which the decomposing number is four and then moving the decomposed impulse response on the time axis by the phase based on the ideal sampling timing of the associated A/D converter 52. When the impulse responses given to the digital filters 56a, 56b, 56c and 56d are assumed to be E_0, E_1, E_2 and E_3, respectively, values constituting the respective impulse responses are determined in a case of Fig. 5, as follows: $E_0 = (P_n, P_{n+4}, \ldots)$, $E_1 = (P_{n-3}, P_{n+1}, \ldots)$, $E_2 = (P_{n-2}, P_{n+2}, \ldots)$ and $E_3 = (P_{n-1}, P_{n+3}, \ldots)$.

[0055] Each digital filter 56 calculates convolution of the values obtained by multiplying the values of the given impulse response by the coefficient based on the phase error in the associated A/D converter 52, and the digital signal output from the associated A/D converter 52, and then outputs the result of the convolution as the corrected signal. That is, in a case where the ideal sampling timings of the A/D converter 52a are assumed to be the reference, the digital filter 56a calculates convolution of the impulse response E_0 and the digital signal; the digital filter 56b calculates convolution of the correction coefficient obtained by multiplying the impulse response E_1 by $e^{(j\omega\tau_1)}$ and the digital signal; the digital filter 56c calculates convolution of the correction coefficient obtained by multiplying the impulse response E_2 by $e^{(j\omega\tau_2)}$ and the digital signal; and the digital filter 56d calculates convolution of the correction coefficient obtained by multiplying the impulse response E_3 by $e^{(j\omega\tau_3)}$ and the digital signal. Then, the digital

filters 56a, 56b, 56c and 56d output the results of the convolution as the corrected signals, respectively. As an example, a transfer function H(z) of the impulse response in the four digital filters 56 is given by the following expression.

[0056] $$H(z) = E_0(z^4) + e^{jw\tau_1} E_1(z^4) z^{-1} + e^{jw\tau_2} E_2(z^4) z^{-2} + e^{jw\tau_3} E_3(z^4) z^{-3}$$

[0057] Fig. 6 shows still another exemplary structure of the digitizer 50 according to the present invention. The digitizer 50 includes N A/D converters 52, N clocks 54, N digital filters 56, the first interleaving unit 64, and the second interleaving unit 66. The A/D converters 52 and the clocks 54 shown in Fig. 6 have the same or similar functions and structures as/to the A/D converters 52 and the clocks 54 described referring to Figs. 2 and 3. Moreover, the digital filters 56 shown in Fig. 6 have the same or similar function and structure as/to the digital filters 56 described referring to Figs. 4 and 5.

[0058] The first interleaving unit 64 generates the first data sequence obtained by arranging digital signals converted by the N A/D converters 52 in a predetermined order and then outputs the first data sequence. Each of the digital filters 56 receives the first data sequence output from the first interleaving unit 64, and calculates convolution of the correction coefficient, that is based on the phase difference between an ideal sampling timing at which the associated one of the N A/D converters 52 is to sample the analog signal and the actual sampling timing at which the associated A/D converter 52 sampled the analog signal, and the first data sequence, thereby generating decimation data in which the number of the contained data units is less than the number of the data units in the first data sequence. The generated decimation data is output. The digital filter 56 may include the decimation data generation unit described referring to Fig. 4. The digital filter 56

generates that decimation data by the same or similar operation as/to the operation described referring to Figs. 4 and 5. The second interleaving unit 66 generates the second data sequence obtained by arranging the data units in the decimation data output from the N digital filters 56 in a predetermined order.

[0059] For example, a case is considered where the A/D converters 52 output data series $x_a(n)$, $x_b(n)$, $x_c(n)$ and $x_d(n)$ of the digital signals, respectively. Then, the first interleaving unit 64 arranges the data units of data series $x_a(n)$, $x_b(n)$, $x_c(n)$ and $x_d(n)$ in a predetermined order without changing the order of data units in each data series, thereby generating the first data sequence $y(4n)$. When the number of the data units in each data series $x_a(n)$, $x_b(n)$, $x_c(n)$, $x_d(n)$ is assumed to be n, the number of the data units in the first data sequence $y(4n)$ is 4n. The digital filters 56 receive the first data sequence $y(4n)$ and then generate decimation data $z_a(m)$, $z_b(m)$, $z_c(m)$ and $z_d(m)$ containing the data units the number of which is less than 4n, respectively. The digital filters 56 generate the decimation data $z_a(m)$, $z_b(m)$, $z_c(m)$ and $z_d(m)$ that are obtained by phase-converting the received data series $x_a(n)$, $x_b(n)$, $x_c(n)$ and $x_d(n)$ to data series in a case where the associated A/D converters perform the sampling at the ideal sampling timings. The second interleaving unit 66 generates the second data sequence obtained by arranging the data units of the decimation data $z_a(m)$, $z_b(m)$, $z_c(m)$ and $z_d(m)$ in a predetermined order.

[0060] For example, when the number of the data units in each data series $x_a(n)$, $x_b(n)$, $x_c(n)$, $x_d(n)$ is assumed to be one, the number of the data units in the first data sequence is four. Each digital filter 56 may receive the first data sequence containing four data units and generate the decimation data containing one data unit so as to output the thus generated

decimation data. In this case, the second interleaving unit 66 generates the second data sequence containing four data units. As described above, according to the digitizer 50 of the present example, even in a case where the sampling rate is reduced by calculation of convolution in the digital filters 56, it is possible to substantially prevent the reduction of sampling rate and is also possible to correct the phase errors in the A/D converters 52. Although the digitizer 50 includes four A/D converters 52 in the present example, it is also possible in the digitizer 50 including N A/D converters 52 to prevent the reduction of the sampling rate and to correct the phase errors in a similar manner.

[0061] Although the present invention has been described by way of exemplary embodiments, it should be understood that those skilled in the art might make many changes and substitutions without departing from the spirit and the scope of the present invention which is defined only by the appended claims.

[0062] As is apparent from the above, according to the digitizer of the present invention, it is possible to correct the phase errors in the A/D converters and to precisely convert the analog signal output from the electronic device to the digital signal. Moreover, according to the testing apparatus of the present invention, it is possible to precisely convert the analog signal output from the electronic device to the digital signal so as to allow the precise determination whether or not the electronic device is defective. Furthermore, the sampling frequency at which the analog signal is sampled can be changed easily.